Machine Learning for Hardware Design Verification with Arm Ltd.

Type of award  PhD Research Studentship  
Department  Computer Science  
Scholarship Details  Minimum £15,009 p.a. for 4 years subject to confirmation and eligibility status plus an industrial top-up of circa £5,000 p.a. depending on experience and performance  
Duration  4 years  
Eligibility  Home/EU applicants only  
Deadline  October 2019  

PhD Topic Background/Description  
This is a prestigious EPSRC iCASE studentship co-funded by Arm Ltd.

This research project will investigate how existing and novel machine learning techniques can be used to improve the results of simulation-based hardware design verification. Areas of improvement may include design coverage (code, functional, or other types), bug discovery probability, the number of simulations required to reach verification goals, the novelty of the internal states the design experiences during simulation, the novelty of the simulation’s outputs, or other areas we may choose during the project. We will prefer techniques that require no human intervention (e.g. to supply insight into the hardware), which are as easy as possible to train, and which can continue to learn from large numbers of data points. To enable this, Arm will provide access to problems and datasets of both academic and industrial interest, as well as collaboration with industrial researchers.

We are offering an opportunity to advance the state of machine learning in an area that is both highly valuable to industry, and not already saturated with competing ML researchers. Hardware verification is the most expensive and time-consuming part of commercial microprocessor development, so improvement in this area is of great commercial interest. Furthermore, the hardware verification process naturally creates large amounts of labelled data in a reproducible way, enabling research on novel datasets without requiring manual data gathering and annotation. However, the data in the hardware verification domain is a challenge to many traditional ML methods because hardware designs often do not have a continuous mapping between input stimuli and output behaviour. We are interested both in practical results (e.g. improvements in rates of bug discovery or the ability to target specific parts of the design during simulation) and in theoretical results (e.g. the creation of new ML algorithms that are especially suited to this kind of data).
Further Particulars

Candidate Requirements
A good 2:1 or first-class degree in Computer Science, Computer Systems Engineering, Informatics, Microelectronic Design or a similar discipline.

Essential:
Excellent programming skills. A good understanding of computer architecture and machine learning techniques will be required for the project.

Desirable
A background in at least one of the following areas: machine learning, processor architecture and design, simulation-based testing, model-based design or testing techniques. You can quickly pick up new programming languages and are willing to learn how to use state-of-the-art professional EDA tools for design verification. A competent presenter, writer and communicator, willing and able to work with our industrial collaborator.

Scholarship Details
The scholarship covers full UK/EU (EU applicants who have been resident in the UK for 3 years prior to 1 September 2019) PhD tuition fees and a tax-free stipend at the current RCUK rate (£15,009 in 2019/20). EU nationals resident in the EU may also apply, but will only qualify for PhD tuition fees.

Informal enquiries
Please email Prof Kerstin Eder (Kerstin.Eder@bristol.ac.uk)
For general enquiries, please email sceem-pgr-admissions@bristol.ac.uk

Application Details
To apply for this studentship submit a PhD application using our online application system [http://www.bristol.ac.uk/study/postgraduate/apply/]

Please ensure that in the Funding section you tick “I would like to be considered for an iCASE funding award from the Computer Science Department” and specify the title of the scholarship in the “other” box below with the name of the supervisor.

Interested candidates should apply as soon as possible.

Closing date for applications 31 July 2019.